IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) ~~An integrated circuit~~ A complementary metal oxide semiconductor (CMOS) device structure comprising:

~~a substrate;~~

~~first-type transistors on said substrate, wherein said first-type transistors comprise first gate conductors and first spacers adjacent said first gate conductors;~~

~~second-type transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer on said first spacers, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors;~~

~~an oxide layer, wherein said oxide layer is on said first gate conductors and said second gate conductors, wherein said first spacers are on said oxide layer, and wherein said etch stop layer is between bottom surfaces of said second spacers and said oxide layer;~~

~~first silicide regions proximate said first spacers of said first-type transistors;~~

~~second silicide regions proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors;~~

~~first-type impurity implants in areas of said substrate adjacent said first spacers of said first gate conductors, wherein said first-type impurity implants are single and non-stepped; and~~

~~second-type impurity implants in areas of said substrate adjacent said second spacers of said second gate conductors, wherein said second-type impurity implants are single and non-stepped, wherein said first-type impurity is spaced closer to said first gate conductors than said second-type impurity is spaced from said second gate conductors~~

an N-type field effect transistor (NFET) gate conductor and a P-type field effect transistor (PFET) gate conductor formed on a substrate;

a first spacer formed on sidewalls of said NFET gate conductor and said PFET gate conductor;

first impurity source/drain implant regions formed, in said substrate, substantially adjacent to outer edges of said first spacer formed on said sidewalls of said NFET gate conductor;

a second spacer formed on sidewalls of said first spacer, which is formed on said sidewalls of said PFET gate conductor; and

second impurity source/drain implant regions, formed in said substrate, substantially adjacent to outer edges of said second spacer formed on said sidewalls of said first spacer, which is formed on said sidewalls of said PFET gate conductor.

2. (Currently Amended) The ~~integrated circuit~~ CMOS device structure according to claim 1, ~~all the limitations of which are incorporated herein by reference, wherein said second spacers are only on said etch stop layer on said first spacers that are adjacent said second gate conductors, and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors~~ further comprising:

an oxide layer formed directly on said sidewalls of said NFET gate conductor and said PFET gate conductor, and directly on areas of said substrate not covered by said NFET gate conductor and said PFET gate conductor.

3-5. (Cancelled).

6. (Currently Amended) The ~~integrated circuit~~ CMOS device structure according to claim [[4]] 2, ~~all the limitations of which are incorporated herein by reference, wherein said first type impurity and said second type impurity comprises source/drain impurities~~ further comprising:

an etch stop layer formed directly on said oxide layer formed directly on said sidewalls of said PFET gate conductor.

7. (Currently Amended) The ~~integrated circuit~~ CMOS device structure according to claim [[1]] 2, ~~all the limitations of which are incorporated herein by reference, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-type field effect transistors (PFETs)~~ further comprising:

silicide regions formed on exposed areas of said oxide layer over said substrate and tops of said NFET gate conductor and said PFET gate conductor.

8. (Cancelled).

9. (Currently Amended) The ~~integrated circuit~~ CMOS device structure according to claim [[8]] 1, ~~all the limitations of which are incorporated herein by reference, wherein said second spacers are only proximate said first spacers that are adjacent said second gate conductors and said second spacers are not proximate said first spacers that are adjacent said first gate conductors~~ wherein a first impurity of said first impurity source/drain implant regions comprises arsenic.

10-11. (Cancelled).

12. (Currently Amended) The ~~integrated circuit~~ CMOS device structure according to claim [[8]] 1, ~~all the limitations of which are incorporated herein by reference, wherein said first-type impurity is spaced closer to said first gate conductors than said second-type impurity is spaced from said second gate conductors~~ wherein a second impurity of said second impurity source/drain implant regions comprises boron.

13. (Currently Amended) The ~~integrated circuit~~ CMOS device structure according to claim [[8]] 3, ~~all the limitations of which are incorporated herein by reference, wherein said first-type impurity and said second-type impurity comprises source/drain impurities~~ wherein said oxide layer comprises a low temperature oxide.

14. (Currently Amended) The ~~integrated circuit~~ CMOS device structure according to claim [[8]], ~~all the limitations of which are incorporated herein by reference, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-type field effect transistors (PFETs)~~ wherein said first spacer and said second spacer comprise nitride films.

15-26. (Cancelled).

27. (Currently Amended) The ~~integrated circuit~~ CMOS device structure according to claim [[26]] 4, ~~all the limitations of which are incorporated herein by reference, wherein said first-type impurity is spaced closer to said first gate conductors than said second-type impurity is spaced from said second gate conductors~~ wherein said silicide regions comprise cobalt silicide.

28-36. (Cancelled).